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A Low-Power Fast Start-Up Crystal Oscillator With an Autonomous Dynamically Adjusted Load

Ming Ding¹, Member, IEEE, Yao-Hong Liu², Senior Member, IEEE, Pieter Harpe³, Senior Member, IEEE, Christian Bachmann, Kathleen Philips, and Arthur Van Roermund⁴, Senior Member, IEEE

Abstract—An energy-efficient fast start-up method for crystal oscillators is presented, which enables aggressive duty-cycled operation of IoT radios to minimize overall power consumption. A digitally controlled crystal oscillator using the proposed start-up technique in 90-nm CMOS is presented. Thanks to the dynamically adjusted load, the negative resistance is boosted, achieving a 13× start-up time reduction and an overall power of 95 μ W for a 24-MHz crystal oscillator at 1 V. A fully autonomous feedback loop detects the oscillators envelop and adjusts the load capacitance at start-up. Thanks to the low-power start-up circuits, both the start-up time and the start-up energy are reduced. In addition, the robustness and versatility of the proposed method is verified by measuring quartz crystals with different frequencies and quality factors, as well as measuring against temperature, supply voltage, and load capacitance variations.

Index Terms—Crystal Oscillator, fast start-up, low-power, IoT, negative resistance, variation-tolerant.

I. INTRODUCTION

WIRELESS sensor nodes (WSN) in Internet-of-Things (IoT) applications require an accurate frequency reference ($\sim$ MHz), which generates a stable reference clock for the PLL to synthesize a carrier and to derive clocks for all other parts of the transceiver SoC. To meet the requirements of IoT radios, high performance is desired for the frequency reference. For instance, low-phase noise is required for IoT radios to meet the requirement of adjacent channel interference and also transmission modulation quality. In addition, robust communication among IoT radios requires a small frequency error as well as high stability over environmental variations. For example, a popular standard such as Bluetooth-Low-Energy (BLE) requires that the transmission frequency error should be within ± 41 ppm (parts per million) of the desired frequency [1]. This leads to a great challenge for on-chip CMOS oscillators, of which the

frequency error is several orders worse [2]. To improve the performance, the oscillator has to consume significantly more power ($\sim$ mW) [3], which is too much for an IoT radio [4]. As a result, crystal oscillators (XO) have been widely used as the frequency reference in IoT radios thanks to their high quality factor (tens of thousands) [5], which enables high performance [6]–[18].

For IoT radios, low-power is essential to achieve long battery life time. To do that, the transceiver is only activated when transmitting or receiving, and disabled to save power when not needed. In this way, the overall system power is reduced without degrading the performance of the radio. But this requires swift start-up behavior for the whole transceiver. This is relatively easier for the transmitter/receiver, the Phase-Locked-Loop (PLL), and the Power-Management-Unit (PMU), whose start-up time is up to a few μ s [4]. Due to the high quality factor, the typical start-up time (T_s) of an XO is, however, relatively long ($\sim$ ms) [6]–[8], [19]–[23]. In applications with a short off-time, the XO can therefore not be switched off and on in time. Thus, it has to be always active, thereby increasing the off-state power of the whole system significantly. In applications with a short on-time, the XO can be switched on and off, but the extra power due to the start-up process can not be neglected. In a duty-cycled radio with a relatively short packet format (for instance the packet length can be as short as 128 μ s in BLE), the power overhead due to the XO start-up process can go beyond 25% [24]. Therefore, a reduction of the XO start-up time of the XO is necessary, and at the same time, the energy overhead to enable a fast start-up should be minimized in order to reduce the overall energy consumption.

The XO start-up time, T_s , not only depends on its quality factor and oscillation frequency, but also on its negative resistance (R_N) [25] and its internal noise [26] at start-up (Fig. 1). Prior-art tried to reduce the start-up time from the following aspects: increase the $|R_N|$ [27], or increase the initial oscillation energy by injecting another signal at the start-up [24], [28], or a combination of the two techniques [29]. Increasing the transconductance (g_m) of the amplifier by providing a higher bias current has been widely adapted to boost $|R_N|$, thus reducing T_s [27]. This method reduces the start-up time, but at the sacrifice of increased start-up power consumption (Fig. 1(a)). Furthermore, the effectiveness of this method is limited by the finite voltage headroom of the devices in the analog circuitry.

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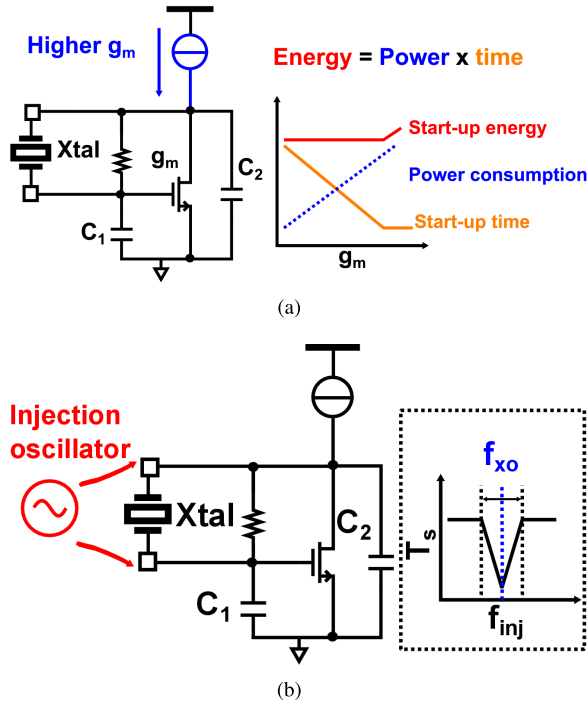


Fig. 1. Illustration of start-up time reduction techniques: increasing g_m (a) and frequency injection (b).

The oscillators presented in [24], [28], and [30] increase their initial oscillation energy to reduce T_s by injecting either a single-tone [28], [30], or a dithered signal [24]. They require a separate RC oscillator, and its frequency has to be calibrated sufficiently close to the resonant frequency of the crystal oscillator (Fig. 1(b)). This is not convenient because the frequency of an RC oscillator is vulnerable to PVT (process, supply voltage, and temperature) variations. [30] is able to overcome most issues, but requires a very good PVT-compensated design in order to guarantee the performance. To make the frequency injection method less sensitive to PVT variations, Chirp Injection (CI) is introduced in [23] and [29] by sweeping the frequency of the injection oscillator over a certain range. However, the improvement in reduction of start-up time is then limited.

In this work, to reduce the start-up time while minimizing the overhead in energy, area and system complexity, a dynamically-adjusted load (DAL) method is proposed [31], [32]. The proposed DAL technique reuses the XO clock once it is available to achieve an automatic control as shown later. The proposed technique achieves a short start-up time ($200\mu s$) and low start-up energy ($<40nJ$).

Section II introduces an application which requests aggressive duty-cycling and thus requires an energy-efficient start-up method for the crystal oscillator. Section III introduces the design considerations of a crystal oscillator. In section IV the implementation of the crystal oscillator is shown. The measurement results will be presented in section V and conclusions will be drawn in section VI.

II. FAST START-UP FOR BLE ADVERTISING

As mentioned, WSNs rely on a small duty-cycling ratio to reduce its average system power consumption. BLE radios

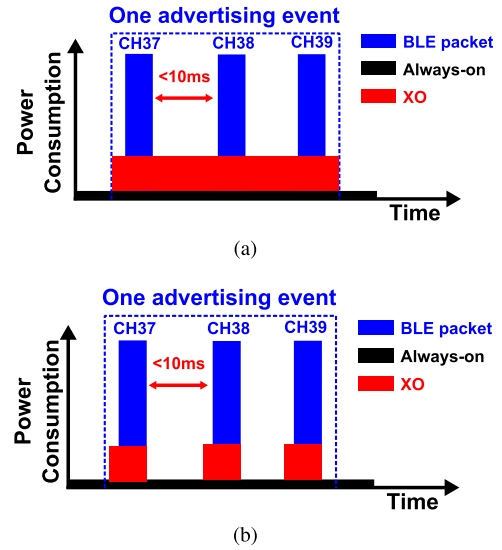


Fig. 2. Illustration of typical BLE advertising (a) and the fast start-up facilitated BLE advertising (b).

has been ubiquitously deployed and easily accessible through battery-powered mobile devices. Small duty-cycling ratio is essential to assure a long battery life time, considering the relatively high power consumption of the radios ($\sim mW$ [4]). In a typical BLE advertising event, the main radio is asleep most of the time, and only activated when broadcasting. During each advertising event, three packets are transmitted over three channels CH37, CH38, and CH39 consecutively, which are located at frequencies of 2402MHz, 2426MHz, and 2480MHz respectively (Fig. 2(a)). The shortest packet has a short format of $128\mu s$. The event interval between two consecutive advertising events is between 10ms to 10.24s, during which the BLE transceiver has sufficient time to be switched off and on to save power. However, within each advertising event, the interval between each packet is no more than 10ms, which is in the same order as typical start-up time of crystal oscillators. For this reason, the XO can not be switched off and has to be always on, consuming power while the BLE transceiver is in off-state. To minimize the power consumption, the time interval between two packets is kept short. However, this increases the chance that two or three advertisement packets will collide with one interference and the whole advertisement event will be blocked.

Alternatively, if the XO start-up time can be reduced sufficiently in a power-efficient way, the XO can also be switched off between two advertising packets (Fig. 2(b)). In this way, the power consumption of the XO can be reduced with a factor of more than $10\times$, leading to significant overall power consumption reduction. Moreover, thanks to the short XO start-up time, the interval between two advertising packets can be increased without introducing power overhead of the XO. In this way, the chance that all the three advertising packets collide with a strong interference is reduce significantly, leading to a better communication quality.

The essential to enable the proposed BLE advertising is a power-efficient start-up approach for crystal oscillator, which will be introduced in the next section.

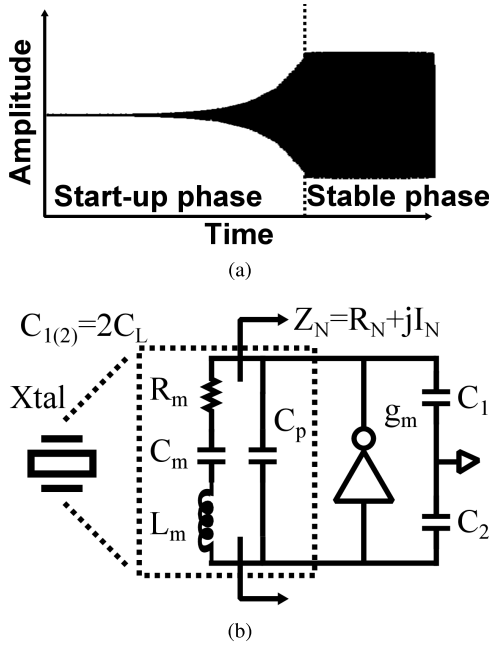


Fig. 3. Start-up behavior illustration (a) and simplified block diagram of a Pierce crystal oscillator with lumped model (b).

III. DYNAMICALLY-ADJUSTED LOAD METHOD FOR FAST START-UP

For a crystal oscillator in a duty-cycled wireless sensor node, once enabled, the process can be roughly divided into two phases: start-up phase and stable phase Fig. 3(a). In the start-up phase, the amplitude of the oscillator ramps up and reaches a stable value in the stable state, in which the crystal oscillator clock can be used by other building blocks of the chip. In the stable phase, the performance of the crystal oscillator should be sufficient for the RF blocks. In addition, the overhead of the start-up method in energy, area and system complexity should be minimized.

Fig. 3(b) shows the simplified block diagram of a popular Pierce crystal oscillator. The crystal quartz can be lumped with L_m , C_m , R_m and C_p as the motional inductor, capacitor, resistor and parallel parasitic capacitor. In order for a crystal oscillator to start-up, the loss of a quartz crystal R_m should be compensated by a negative resistance R_N , which is given by [25]

$$|R_N| = \frac{g_m C_1 C_2}{(g_m C_p)^2 + \omega^2 (C_1 C_2 + C_2 C_p + C_1 C_p)^2}, \quad (1)$$

where $C_{1(2)} = 2C_L$. In the start-up phase, the key to reduce the start-up time is to increase $|R_N|$ as much as possible. For a crystal oscillator, $C_{1(2)} \gg C_p$, and R_N can be approximated by $-\frac{g_m}{(2\omega C_L)^2}$, where ω is the oscillation angular frequency and load capacitance C_L equals $0.5C_{1(2)}$. It can be seen that R_N is approximately quadratic to $1/C_L$, so reducing C_L is very effective to obtain a higher $|R_N|$ at start-up. Considering that g_m can be limited by the voltage headroom of the analog circuits [27], reducing C_L can overcome the bottleneck of voltage headroom to boost R_N . This gives an additional advantage for low supply voltage designs in modern CMOS technologies. In addition, the required minimum g_m for a crystal oscillator

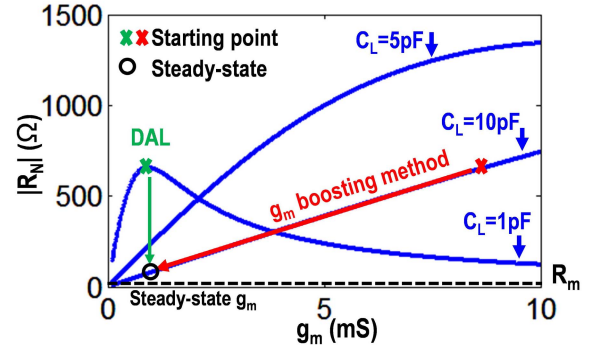


Fig. 4. Comparison of g_m method and DAL method.

to start-up is proportional to $R_m(2\omega C_L)^2$ [25], indicating that less power is needed for crystal oscillators with smaller C_L for start-up. Therefore, in the start-up phase, a smaller C_L is desired to reduce both start-up time and power consumption.

In the stable phase, the frequency pulling factor ($\sim \frac{C_m}{2C_p + 2C_L}$) [25] indicates the difference between the real oscillation frequency and the intrinsic resonant frequency of a quartz crystal. A large C_L is preferred for a quartz crystal as it results in a small frequency pulling factor and thus a small frequency error, which is desired for radio. In addition, a large C_L also improves stability over environmental variations.

Reference [17] proposes to increase R_N by isolating the parasitic shunt capacitor C_p of the quartz crystal during start-up. Reference [18] proposes to increase R_N by programming the load capacitance to one small value and to another large value after a delay, but did not provide insight how to optimize start-up time and energy and lacks the feedback loop to automatically increment the load capacitor C_L . In practice, the relation between R_N and g_m is more complicated (eq. 1), which is illustrated in Fig. 4. The required g_m of a crystal oscillator is proportional to $(\omega C_L)^2$ [25]. For example, for a crystal oscillator with 10pF load capacitance, g_m has to be relatively high for fast start-up. Compared to the g_m method, the DAL method temporarily sets the load capacitance to a smaller value such that during start-up a much smaller g_m is necessary to achieve the same $|R_N|$. In this way, the DAL method is more energy-efficient compared to the g_m method. For each load C_L , $|R_N|$ increases with g_m within a certain range. However, if the g_m is larger than its value where $|R_N|$ is optimal, $|R_N|$ will decrease due to the g_m -boosted effect on C_p , which is not desired (Fig. 4). It is worthwhile to mention that a larger C_L leads to a larger theoretical peak $|R_N|$ (Fig. 5), but at the cost of much higher power as mentioned before.

In addition, to quantitatively analyze the start-up time T_s and start-up energy E_s for a given crystal oscillator, they are computed and simulated versus the transconductance g_m and load capacitance C_L in Matlab. The start-up time for a given crystal oscillator can be estimated as [26], [29]:

$$T_s = \frac{2L_m}{|R_N| - R_m} \ln \left(\frac{0.9\omega C_T V_{DD}}{|I_{M(0)}|} \right), \quad (2)$$

where C_T is defined as $\frac{C_1 C_2}{C_1 + C_2} + C_p$, V_{DD} is the supply voltage and $I_{M(0)}$ is the amplitude of the current in the node containing

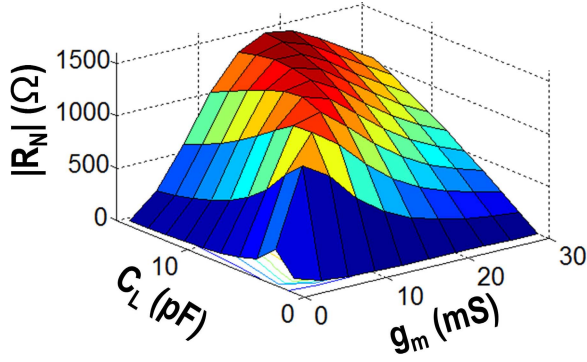


Fig. 5. Simulated $|R_N|$ versus g_m and load capacitance C_L .

the quartz crystal. T_s is the time to reach steady-state, and $\frac{2L_m}{|R_N| - R_m}$ equals the time constant, τ , of the amplitude exponential growth [26]. The relationship between the start-up time T_s and g_m and C_L is calculated and shown in Fig. 6. For each load capacitance, there is an optimum $g_{m,opt}$ that results in a minimum start-up time T_s . This is because $|R_N|$ is maximal at $g_{m,opt}$. T_s increases at a smaller or larger g_m due to the decrease of the $|R_N|$. When $|R_N|$ approaches R_m , T_s goes up rapidly. Once $|R_N|$ drops below R_m , the crystal oscillator will fail to start up. The optimum value for g_m , $g_{m,opt}$, is expressed as [25]:

$$g_{m,opt} = \omega \left(C_1 + C_2 + \frac{C_1 C_2}{C_p} \right). \quad (3)$$

The equation shows that $g_{m,opt}$ is proportional to its load capacitance $C_{1(2)}$ (Eq. 3). Therefore, for crystal oscillators with smaller load capacitance C_L , a smaller g_m is needed. The start-up time at $g_{m,opt}$ can be expressed as:

$$T_{s,opt} = \frac{2L_m}{1/(2\omega C_p(1 + \frac{(C_1+C_2)}{C_1 C_2} C_p)) - R_m} \ln \left(\frac{0.9\omega C_T V_{DD}}{|I_{M(0)}|} \right). \quad (4)$$

The theoretical maximum $|R_N|$ for crystal oscillators with smaller C_L is lower than that with higher C_L (Fig. 4 and Fig. 5). As a result, the $T_{s,opt}$ for crystal oscillators with smaller C_L is larger than that with larger C_L (Fig. 6). The measured start-up time of this realized crystal oscillator (two points as shown in Fig. 6) is close to the calculated optimum point for $C_L = 2\text{pF}$.

With the calculated start-up time, the total energy during the start-up is further calculated as follows:

$$\begin{aligned} E_s &= V_{DD} \times I_d \times T_s \\ &= \frac{V_{DD} L_m}{V_{OV}} \frac{g_m}{|R_N| - R_m} \ln \left(\frac{0.9\omega C_T V_{DD}}{|I_{M(0)}|} \right), \end{aligned} \quad (5)$$

where V_{OV} is the overdrive voltage of the transistor that generates the negative resistance and I_d is the current consumption of the crystal oscillator, which can be estimated as $g_m V_{OV}/2$ assuming V_{OV} is constant. As shown in Fig. 7, for each load capacitance C_L , there is an optimum range for g_m that results in a minimum start-up energy. Within this range, as g_m increases, start-up time T_s decreases, and the start-up energy remains the same. When combining Fig. 6 and Fig. 7, it can

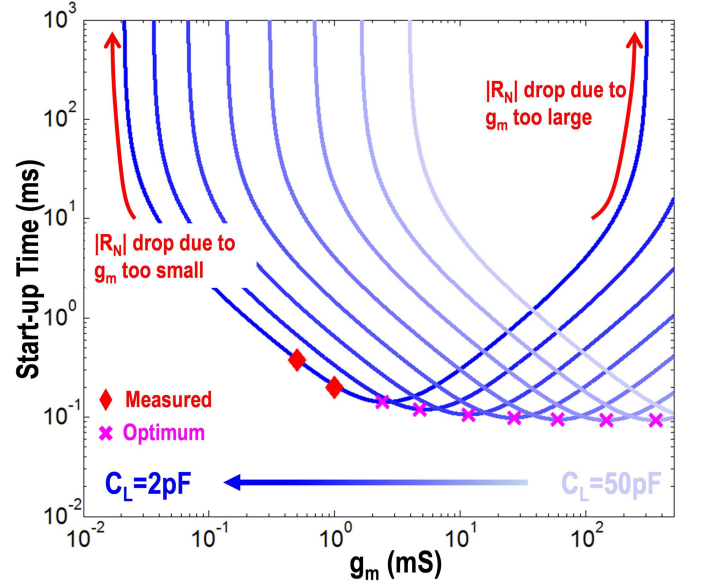


Fig. 6. Simulated start-up time T_s versus g_m and load capacitance C_L . $L_m = 5.8\text{mH}$, $R_m = 20\Omega$, $\omega = 2\pi \times 24\text{M rad/s}$, $V_{DD} = 1\text{V}$, $I_{M(0)} = 5\text{nA}$.

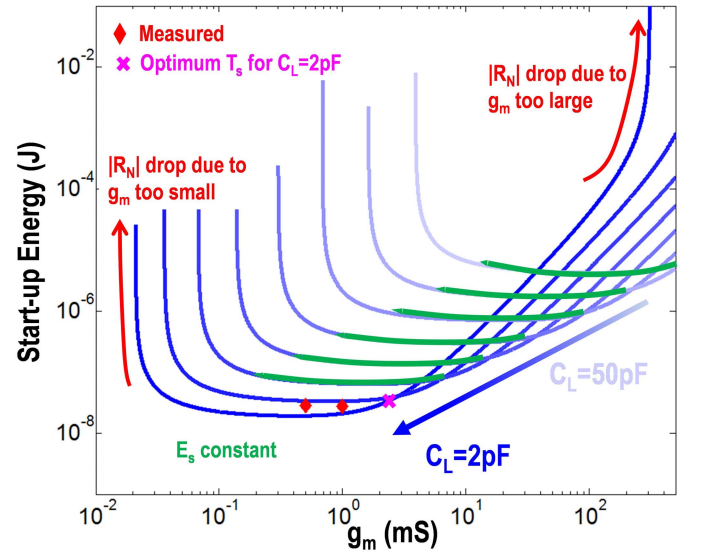


Fig. 7. Simulated start-up energy E_s versus g_m and load capacitance C_L . $L_m = 5.8\text{mH}$, $R_m = 20\Omega$, $\omega = 2\pi \times 24\text{M rad/s}$, $V_{DD} = 1\text{V}$, $I_{M(0)} = 5\text{nA}$.

be observed that if the circuit is optimized for start-up time T_s , this leads to a near-optimal start-up energy E_s directly. However, a circuit optimized for start-up energy E_s is not necessarily achieving the optimum start-up time T_s . As g_m further increases, due to the $|R_N|$ degradation, see Fig. 4, the start-up time will increase, and thus the start-up energy will increase. The minimum start-up energy for a crystal oscillator with $C_L = 2\text{pF}$ is approximately $200\times$ lower than that with $C_L = 50\text{pF}$. This gives an indication that start-up with smaller C_L can save energy significantly, which is also shown in Fig. 7.

To optimize both the start-up performance and the frequency stability of the stable state, in this work, an XO with a dynamically-adjusted load (DAL) technique is proposed, minimizing the C_L in the start-up phase at first for fast start-up and thereafter incrementing C_L for stable operation in the

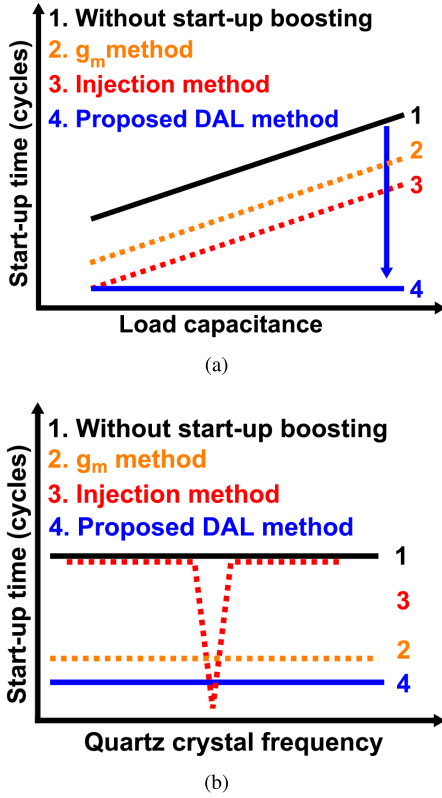


Fig. 8. Comparison of various start-up approaches with respect to load capacitance (a) and XO frequency (b).

stable phase. As a result, both the start-up time and the start-up energy can be reduced. In the stable phase, the operation condition (e.g., load capacitance) of the crystal oscillator is correctly configured, and the performance in the stable phase is not sacrificed as shown later.

In the proposed method, the load capacitance at the start-up remains similar regardless of the C_L used in the stable phase of different quartz crystal (Fig. 8(a)). This allows a larger C_L to be employed to improve the tolerance to the parasitics changes without increasing the start-up time. In addition, for the frequency injection method, when the frequency of the crystal oscillator is changed (for example, due to a different quartz frequency), the injection oscillator has to be re-designed, otherwise it will not be effective in reducing the start-up time (Fig. 8(b)). The proposed method is less sensitive to such frequency variations since no frequency injection is required.

IV. IMPLEMENTATION OF THE CRYSTAL OSCILLATOR

Fig. 9 shows the block diagram of the fast start-up XO with the proposed DAL as well as an illustration of its start-up behavior in the time domain. It consists of a Pierce oscillator as its core, a reconfigurable bias current circuitry, two switched capacitor banks ($C_{1a(2a)}$), and a feedback loop to implement the DAL. The proposed dynamically-adjusted load method is implemented through the feedback loop, which works as follows (Fig. 9(b)): $C_{1a(2a)}$ is reduced to minimum to boost the negative resistance R_N , facilitating a fast start-up. Therefore, the amplitude of the oscillator is able to ramp up in a short time. A clock detector in the feedback loop is continuously

monitoring the amplitude of the oscillator, and will decide if the crystal oscillator has a sufficient output swing to provide a clock for the digital circuit. If so, a finite state machine (FSM) will automatically increase $C_{1a(2a)}$ to the targeted value. During the start-up, the frequency of the crystal oscillator deviates from the nominal frequency (maximum hundreds of ppm as shown later) because of the frequency pulling effect due to the varying capacitor value ($C_{1a(2a)}$). This frequency offset error is not a problem because it is still sufficient for operation of the digital circuits in the feedback loop. Besides, once $C_{1a(2a)}$ is set, the oscillator frequency settles to the correct value automatically after a few μs delay. After this latency the RF circuits can be switched on, as the oscillator is fully settled then. Note that the whole start-up process is fully autonomous without requiring an extra oscillator or sequence. This makes it possible to implement the DAL method with only an enable signal, which is very convenient for many IoT applications. In addition, it is worthwhile to mention that, thanks to the switched capacitor bank, the frequency of the oscillator can be trimmed by configuring the switched capacitor banks. In this way, the proposed DAL is compatible with the implementation of a digitally-controlled XO (DCXO), which is desired for many WSN [33]. In those applications, cheap quartz crystals are preferred, however, they usually have larger frequency variations and require frequency trimming.

A. Oscillator Core

The Pierce oscillator core uses an NMOS transistor to implement the negative g_m for negative resistance. The bias current circuit provides a reconfigurable current for the oscillator from a $20\mu A$ bias current input to compensate the variations due to process spread, environmental fluctuation, or different quartz crystals. Since the noise of the crystal oscillator will be up-converted when it is used as the reference clock for a PLL, the noise of the crystal oscillator should be optimized. The ratio of the current mirror is minimized to reduce the noise contribution from the current mirror devices. The resistor R_b is set to $40k\Omega$ to bias the NMOS while avoiding loading the crystal quartz. The trip-point of the inverter-based buffer is optimized to equal the DC level of the crystal core, so that the gain of the inverter is maximized. As a result, it can amplify the signal of the oscillator core to rail-to-rail so that the input-referred noise of the inverter is minimized.

The load capacitors $C_{1(2)}$, equal to $2C_L$, consist of two parts: on-chip switched capacitor banks $C_{1a(2a)}$ and the parasitics $C_{1b(2b)}$ due to on-chip routing, bonding and packaging, and PCB routing. $C_{1a(2a)}$ is programmable up to $16pF$, and is implemented with a 6b switched capacitor bank (Fig. 10). $C_{1b(2b)}$ is about $4pF$, resulting in a maximum $(16pF+4pF)/2 = 10pF$ load capacitance. At start-up, the capacitor bank is switched dynamically, which disturbs the oscillation amplitude of the crystal oscillator. Assuming the charge on the capacitor stays the same when switching a capacitor, the voltage variation ΔV at nodes XOP and XON due to switching of the capacitor can be estimated as:

$$\Delta V = \frac{V_0}{1 + C_0/C_u}, \quad (6)$$

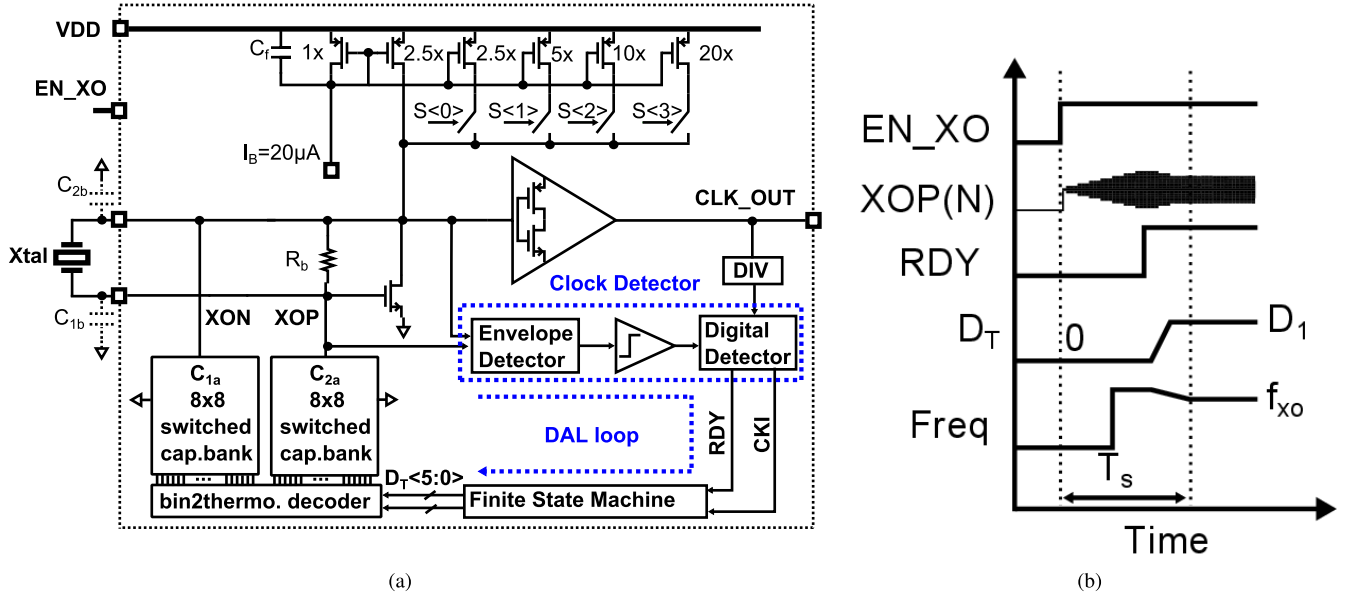


Fig. 9. Block diagram of the crystal oscillator with autonomous dynamically-adjusted load (DAL) (a) and a waveform illustration (b).

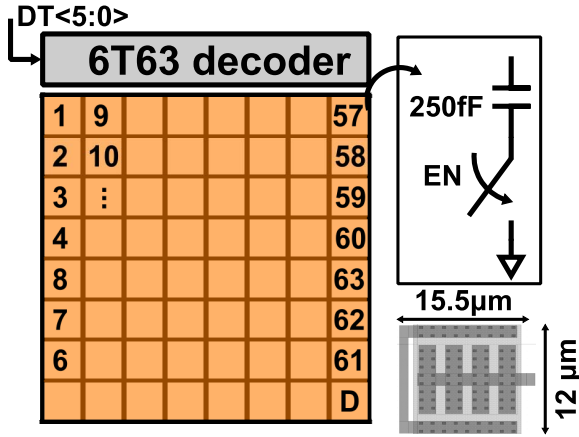


Fig. 10. The 6b thermometer-encoded capacitor bank.

where V_0 and C_0 are the voltage and capacitance of the capacitor before switching the capacitor, and C_u is the added capacitance. Depending on the switching moment, C_0 can be any value between 4pF and 20pF, while V_0 should be around $0.5V_{DD}$ because the capacitor is switched at the edge of the clock. The switching induced voltage variation ΔV starts with a relatively larger value ($\frac{V_0}{1+(C_{1b}+C_{2b})/C_u}$) at the beginning and then gradually reduces to a smaller value ($\frac{V_0}{1+(C_{1a}+C_{2a}+C_{1b}+C_{2b})/C_u}$) at the later stage of the start-up. Theoretically the unit capacitor should be as small as possible to minimize the voltage variation. However, this increases the complexity of the capacitor bank and therefore the parasitics. Therefore, in this work, a 6b capacitor bank is chosen and this results in a 250fF LSB size. In addition, the capacitors are switched at the zero crossing point of XOP and XON when the differential change in the load capacitors is minimum, so that the differential switching induced voltage variation is also reduced. The unit capacitor cell is implemented using a MIM (Metal-Insulator-Metal) capacitor in series with a complementary switch (Fig. 10).

The switches of the capacitor bank are carefully sized to trade-off between the quality factor of the capacitor bank and the induced parasitics. In this work, the switches are sized relatively large ($15\mu\text{m}/0.1\mu\text{m}$) to assure sufficient quality factor (700). This is at the cost of an increase of the off-state parasitic capacitance (1.26pF in total). Each time at start-up, by configuring the final settled value of $C_{1(2)}$, the frequency of the oscillator in the stable phase is trimmed automatically. The tuning accuracy in this work is $<7\text{ppm}$ with a tuning range larger than $\pm 50\text{ppm}$, which is sufficient for many IoT applications, for example, BLE or IEEE802.15.4.

B. Dynamically-Adjusted Load Circuits

A feedback loop, which implements the dynamically-adjusted load method, performs the detection function to monitor the oscillator amplitude and determines the moment to increase the load capacitance. It consists of a clock detector circuit and an FSM (Fig. 9(a)). The clock detection circuit includes two parts (Fig. 11): an amplitude detector which is composed of an envelope detector (ED) in series with a comparator, and a digital clock detector. The envelope detector and the comparator are continuously monitoring the amplitude of the crystal oscillator, by comparing with a reference voltage. Once the oscillator amplitude exceeds this threshold, the comparator output will trigger the FSM to generate a 6b tuning code that gradually ramps up the switched capacitor bank to the final value.

The envelope detector extracts the amplitude information of the sinewave of the crystal oscillator. It uses a pseudo-differential architecture as shown in Fig. 11(a) to suppress the common-mode variations. The resistor R_e and the capacitor C_e are set to 55kohm and 2pF respectively, resulting in a 700kHz bandwidth, which effectively attenuates the high frequency components. This generates a relatively smooth output of the envelope detector, with an acceptable delay in the DAL loop (a few μs).

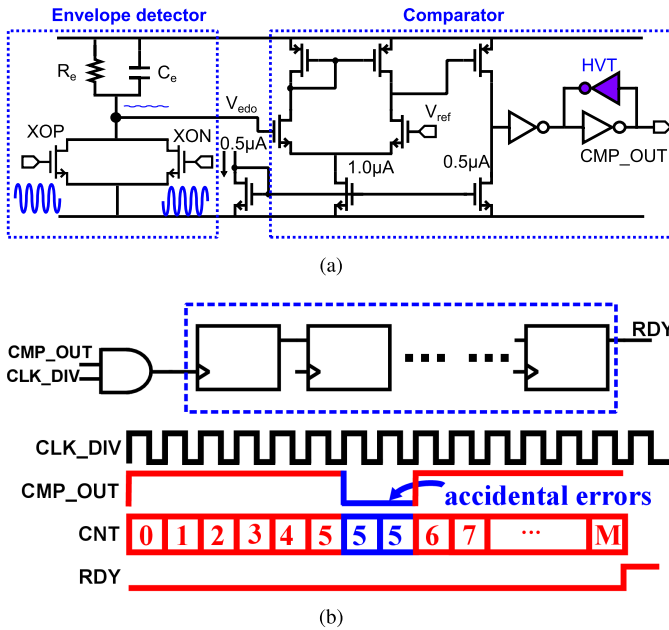


Fig. 11. The amplitude detection circuitry (a) and the digital detection circuitry (b).

The comparator is continuously comparing the ED output with a reference voltage. It consists of a three-stage op-amp and a latch. The input stage consumes only $1\mu\text{A}$, and the second stage $0.5\mu\text{A}$. The bandwidth is set as 4MHz , resulting in a negligible delay compared to that of the envelope detector. The third stage is an inverter, providing a rail-to-rail output. The voltage V_{edo} at the comparator input has ripples due to the limited high frequency attenuation of the envelope detector, resulting in glitches at the comparator output, which is not desired. In order to overcome this issue, a digital Schmitt trigger is implemented using a cross-coupled latch (Fig. 11(a)) [34]. The hysteresis of the latch is designed to be higher than the ripple at the ED output to avoid oscillation at the comparator output. The reference voltage of the comparator uses a resistor-ladder based voltage divider from the bias circuits.

After the comparator indicates sufficient oscillation amplitude, a digital clock detection circuit is further used to ensure that the clock quality is sufficient before the load adaptation is initiated (Fig. 11(b)). The logic filters out accidental errors of the comparator, and will only proceed if M correct cycles are counted. The counter operates at a lower frequency (divided by 4), resulting in an acceptable delay ($\sim 1\mu\text{s}$). Once the RDY becomes active, the FSM starts to function. It generates a 6-bit tuning code D_T which increments from 0 to the desired value, to control the capacitor banks. The operation frequency of the FSM is kept relatively low (divided by 4), slowing down the switching transient meanwhile with an acceptable delay (maximum $10\mu\text{s}$). Moreover, the capacitor bank is thermometer-encoded instead of binary-encoded. In this way, the voltage fluctuations of the crystal oscillator during this transient are minimized, avoiding as much as possible clock glitches. In a dual-mode crystal oscillator [9], a long transition time ($130\mu\text{s}$) is used during switching between two modes. This is to assure that no glitches will happen because the clock

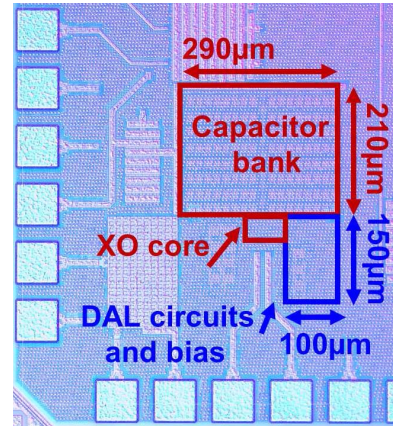


Fig. 12. Chip photo.

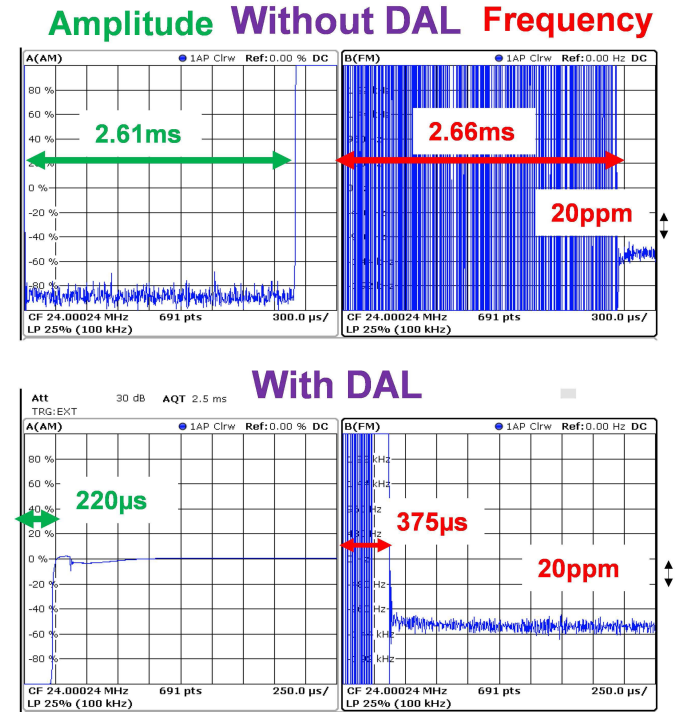


Fig. 13. Measured start-up behavior in two scenarios: without, with DAL.

has to be proper in both modes. In this work, at the start-up of the oscillator, a relative short transient time ($\sim 10\mu\text{s}$) is used to compromise between delay and possibility of glitches. After the start-up of the oscillator, the crystal oscillator clock will be used for the other circuits of the chip.

In practice, the circuits that are used for fast start-up (including the ED, the comparator, and the reference voltage) can be disabled once the output of the FSM increments to the expected value. This is not implemented in this chip.

V. MEASUREMENTS

To verify the functionality of the proposed DAL method, a prototype of the test chip is implemented in 90nm LP CMOS as shown in Fig. 12. The core area is 0.072mm^2 , including the load capacitor (84%) and the feedback loop to implement the DAL method (10%). A 24MHz quartz crystal, of which

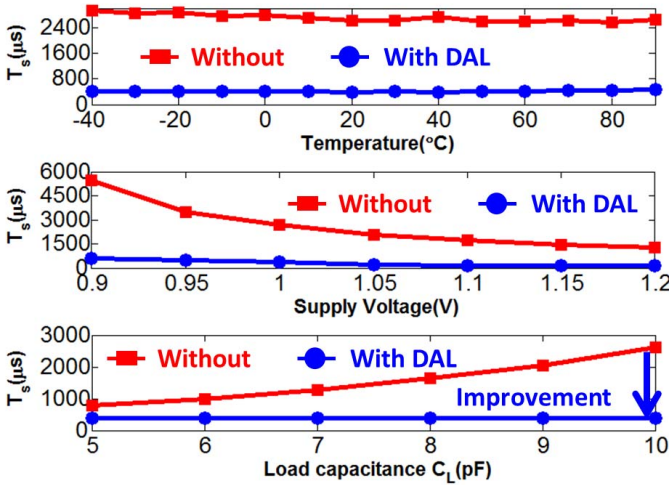


Fig. 14. Measured start-up time with respect to temperature, supply voltage and load capacitance variations.

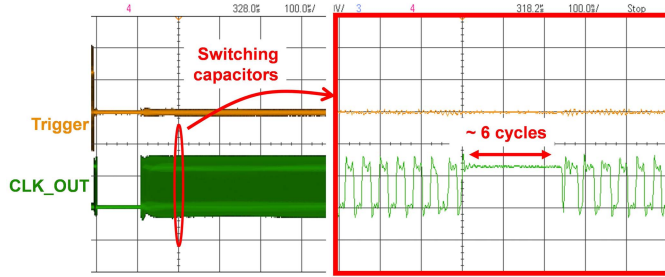


Fig. 15. Measured hang-up of the output clock during startup.

the estimated quality factor is 54800, is used to verify the functionality of the chip. At 1V, the chip consumes $95\mu\text{W}$ in the steady state and the circuits to implement the DAL method consume $9\mu\text{W}$ extra at the start-up.

The start-up time is measured as follows: the CLK_OUT is measured utilizing the amplitude/frequency demodulation feature of the FSV Rohde&Schwarz signal analyzer, because it is not desired to measure the amplitude of the oscillator directly by probing due to the large capacitive load (namely tens of pF). In this way, the amplitude and frequency of the output clock can be measured without disturbing the load capacitance of the crystal oscillator. Fig. 13 shows the measured amplitude (left part) and frequency (right part) of the XO output CLK_OUT during the start-up, which comprises three phases. Before the oscillator starts up, the amplitude of CLK_OUT is low and the demodulated frequency is very noisy. Once the XO starts up, CLK_OUT will be detected but its frequency is not yet accurate and stable. After the load capacitor $C_{1(2)}$ is correctly settled, the frequency will be stable. The start-up time is defined as the duration for the frequency to settle within $\pm 20\text{ppm}$ from the target frequency, which is well within the requirement of many IoT standards, e.g. BLE ($\pm 41\text{ppm}$) and IEEE802.15.4 ($\pm 40\text{ppm}$) [1]. Without any start-up technique, the oscillator takes 2.66ms to start up. With the DAL technique only, the frequency can settle within $375\mu\text{s}$, resulting in a $7\times T_s$ reduction. By slightly increasing the power to $146\mu\text{W}$ for a higher g_m of 1mS ,

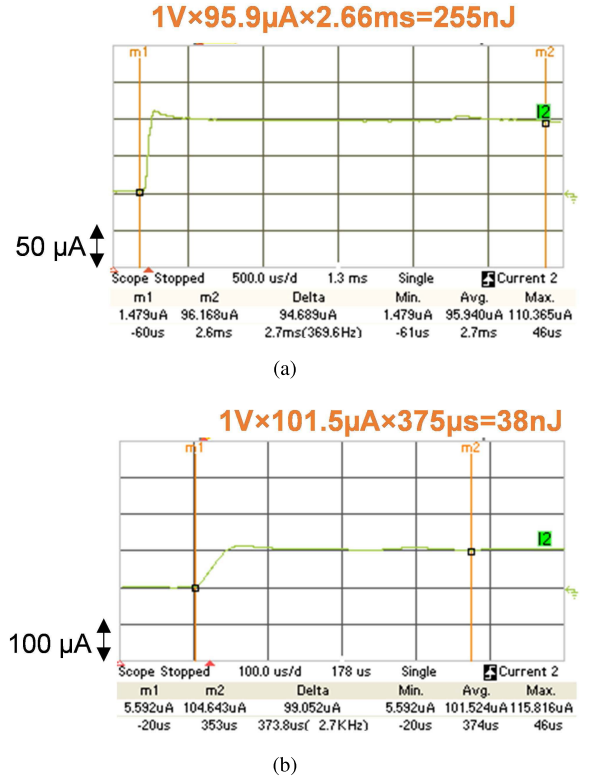


Fig. 16. Measured current profile without boosting technique (a), and with DAL (b).

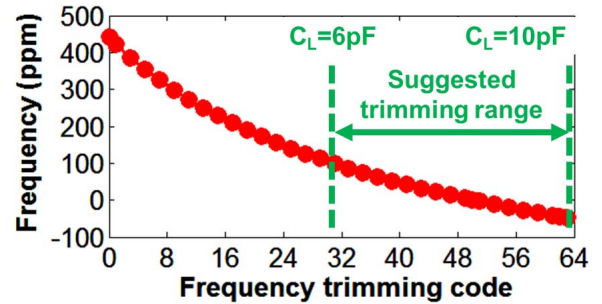


Fig. 17. Measured frequency trimming performance.

TABLE I
START-UP MEASUREMENTS USING THREE DIFFERENT QUARTZ CRYSTALS

	Crystal size (mm ³)	Frequency (MHz)	Start-up time (ms)		
			Without	DAL	DAL + g_m
Crystal No. 1	5.0×3.2×1.0	24	2.6	0.37	0.2
Crystal No. 2	5.0×3.2×1.0	32	4.1	0.63	0.38
Crystal No. 3	4.0×2.5×0.8	24	4	0.67	0.37

the frequency can settle in $200\mu\text{s}$, resulting in $13.3\times T_s$ reduction. If only the g_m method is applied, it gives roughly $2\times$ start-up time reduction. The g_m can be further increased by increasing the power consumption, but that is not desired. As shown in Fig. 15, a temporary hang-up of the output clock CLK_OUT occurs during the startup of the oscillator. This is caused by the switching of the capacitor bank, which produces a temporary internal common mode voltage drop on nodes XOP and XON. The oscillator core is still running

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	[21] JSSC'12	[29] JSSC'16	[24] ISSCC'16		[30] JSSC'18	[23] JSSC'18	This work	
Technology (nm)	65	180	65		65	65	90	
Core area (mm ²)	0.15	0.12	0.08		0.09	0.023	0.072	
Supply (V)	1	1.5	1.68		1.0	0.35/0.7	1.0	
Frequency (MHz)	26	39	24		10	24	24	
Load capacitance, C _L (pF)	8	8	6	9	9	6	10	
Steady-state power (μW)	2180	181	393	693	23.6	31.8	95	
Start-up time (μs)	3200*	158*	64*	435*	11.3*	400*	375**	200**
Start-up time (cycles)	83200	6162	1536	10440	113	9600	9000	4800
Total start-up energy (nJ)	6976	349	-		13.5	14.2	38	36.7
T _s variation with Temp.	-	<7%	±35%	±20%	3%	7.5%	26.6%	27.5%
Temperature range (°C)	-	-30 to 125	-40 to 90		-40 to 85	-40 to 90	-40 to 90	
Crystal size (mm×mm)	-	-	3.2×2.5	2.0×1.6	11.4×4.7, 3.2×2.5	3.2×2.5	5.0×3.2	
Fast start-up Technique	None	CI + g _m	Dithered injection		Precisely-Timed injection	3-stage g _m + SSCI	DAL	#DAL + g _m
Extra oscillator required	-	Yes	Yes		Yes	Yes	No	

* start-up timer defined as the time it takes for the oscillation amplitude to reach 90% of its steady-state value

**start-up time defined as the time it takes for the oscillation frequency to settle within ±20ppm

In DAL + g_m method, the power consumption for start-up is increased, with respect to DAL only, to 146μW

correctly, but the common-mode shift moves the oscillator signal temporarily out of the trip-point of the inverter buffer, thus resulting in a hang-up of the output clock CLK_OUT for approximately 6 cycles. This is not a problem because this only happens at the start-up when switching capacitors. After that, the capacitor digital control bits are static and no hang-up will occur. In addition, the start-up time measurements are repeated with temperature variations, supply voltage variations and load variations (Fig. 14). With the temperature swept from -40°C to 90°C, the measured start-up time variation is 13% and 26.6% without/with DAL. No frequency trimming is performed and the frequency drifting is less than 20ppm. With a swept supply voltage from 0.9V to 1.2V, the measured start-up time variation is 66%. The performance fluctuation is mainly due to the g_m variation. Moreover, with the large load capacitance varying from 5pF to 10pF, a very stable start-up performance (3%) is achieved. This matches with the expected behavior as shown in Fig. 8(a).

To measure the energy during the start-up process, the real-time current profile of the supply voltage is captured using Keysight current analyzer N6705B LXI, as shown Fig. 16. The measured total energy is calculated based on the measured real-time current. With DAL enabled, the measured total start-up energy is reduced from 255nJ to 38nJ. Thanks to the low-power circuit for start-up, the energy overhead is minimized, leading to an approximately 6.7× start-up energy reduction with a 7× start-up time reduction. When increasing g_m and DAL are both applied at start-up, the start-up time reduction is further reduced to 13×. But as mentioned before, increasing only the g_m reduces the start-up time at a higher power consumption. Thus, the start-up energy reduction is similar as that with DAL applied only (6.9×). The energy of the voltage reference generation is not included because it is located in a separate power domain with a separate supply voltage. With it included, the total start-up energy increases by only 1.5nJ and 0.8nJ in the scenario with DAL only and with both DAL and g_m.

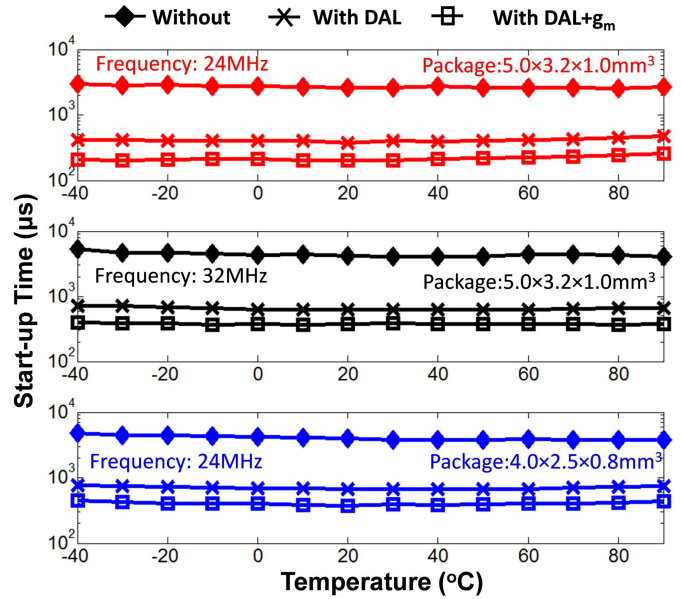


Fig. 18. Measured crystal oscillator start-up variations over temperature for three different crystal devices.

The frequency tuning range is measured using the Agilent 53230A frequency counter. Each frequency is averaged over 1000 measurements. The measured frequency tuning range is roughly [-48ppm, +440ppm] (Fig. 17), among which [-48ppm, +102ppm] is suggested to be used for frequency trimming, because further reducing the load capacitance will degrade the performance of the XO. The averaged frequency trimming accuracy is 5ppm, which is sufficient for many IoT applications, such as BLE or IEEE802.15.4. It achieves -141dBc/Hz measured phase noise at 100kHz frequency offset, which is good enough for most IoT applications, such as BLE or IEEE802.15.4.

To verify the validity of the proposed method, the measurement is repeated using three different quartz crystals with

different package size, frequency or quality factor as shown in Table I. Crystal oscillators with higher quality factor quartz have longer start-up time. But the proposed DAL method can effectively reduce the start-up time for all the three crystal oscillators, and with both DAL and g_m applied, the start-up time can be further reduced. In addition, the start-up time measurements against temperature variations are also repeated for all three crystal oscillator as shown in Fig. 18. It can be seen that the measured start-up time is also stable over temperature variations.

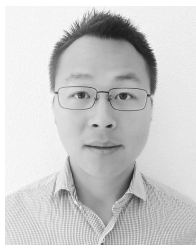
The performance of this work is summarized in Table II. Note that the absolute start-up time/energy can be influenced by many factors such as the crystal quality factor and package size. Nonetheless, the proposed method can improve both the start-up time and start-up energy thanks to its low-power start-up circuit. In addition, the start-up circuits are fully autonomously operated and insensitive to crystal oscillator frequency, making them suitable for future IoT applications.

VI. CONCLUSION

A fast start-up crystal oscillator with a dynamically-adjusted load in 90nm CMOS is demonstrated. The proposed method features a fully autonomous operation, and has negligible overhead in power. Thanks to the DAL method, this work improves both the start-up time and the start-up energy, which is very attractive for future IoT applications.

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